Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) Method of forming an interconnect structure comprising the steps of:

depositing a dielectric layer;

forming a hard mask over the dielectric material [[;]] , wherein the hard mask comprises:

a layer of silicon carbide (SiC) material overlying the dielecteric layer; and

a layer of oxide the silicon carbide material;

etching trenches in the dielectric material;

depositing a liner material over the hard mask and within the trenches; and

overfilling the trenches with a conductive material;

~~characterized by:~~

performing a first chemical mechanical polishing process to remove conductive material which is atop the liner, thereby exposing the liner;

removing that portion of the liner which is atop the hard mask[[;]] using a process selected from the group consisting of reactive ion etch (RIE) and a Gas Cluster Ion Beam (GCIB), leaving conductive material protruding; and

removing ~~a first portion of the hard mask~~ the layer of oxide using a wet etch process, ~~thereby~~ leaving ~~in place a second portion of the hard mask~~ the layer of silicon carbide, followed by ~~; and~~

performing a touch-up polishing process to remove conductive material ~~and liner material~~ protruding from the trenches.

2. (original) The method of claim 1, wherein the dielectric layer comprises a low-k material.

3. (original) The method of claim 1, wherein the dielectric layer comprises an ultralow-k material.

4. (currently amended) The method of claim 1, wherein ~~the hard mask comprises~~:

~~a layer of silicon carbide material atop the dielectric layer; and~~

~~a layer of oxide atop the layer of silicon carbide~~

the layer of silicon carbide material has a thickness in the range of 1000-5000A.

the layer of oxide has a thickness in the range of 1000-5000A.

5. (original) The method of claim 1, wherein the conductive material is copper.

6. (canceled) ~~The method of claim 1, wherein the portion of the liner which is atop the hard mask is removed by a reactive ion etch (RIE) or a Gas Cluster Ion Beam (GCIB) process.~~

7. (canceled) ~~The method of claim 1, wherein the portion of the liner which is atop the hard mask is~~

~~removed by a second chemical mechanical polishing process.~~

8. (canceled) ~~The method of claim 1, wherein the first portion of the hard mask comprises oxide.~~

9. (currently amended) The method of claim [[8]] 1, further comprising the step of:

ensuring that the layer of oxide ~~portion of the hard mask~~ is thick enough such that the topographical variations after the first chemical mechanical polishing process and liner removal are entirely within the oxide portion of the hard mask.

10. (currently amended) The method of claim [[8]] 1, wherein the layer of oxide has a thickness in the range of 50 – 5000A.

11. (currently amended) The method of claim 1, wherein the layer of silicon carbide material has a thickness in the range of 50 – 5000A ~~the second portion of the hard mask comprises a silicon carbide (SiC) material~~.

12. (canceled) ~~The method of claim 1, wherein:~~

~~the first portion of the hard mask comprises oxide; and~~

~~the second portion of the hard mask comprises a silicon carbide (SiC) material.~~

13. (currently amended) The method of claim 1, wherein the touch-up polishing process comprises using ~~uses~~ an abrasive-free or low-abrasive polish to obtain a very high selectivity between the conductive material and the second portion of the hard mask.

14. (canceled) ~~Method of forming an interconnect structure comprising the steps of:~~

~~depositing a dielectric material;~~

~~forming a hard mask over the dielectric material;~~

~~etching trenches in the dielectric material; and~~

~~overfilling the trenches with a conductive material;~~

~~characterized by:~~

~~performing a first chemical mechanical polishing step;~~

~~then, performing a wet etch step; and~~

~~then, performing a second chemical mechanical polishing step.~~

15. (canceled) ~~The method of claim 14, wherein at least a portion of the hard mask is left substantially intact.~~

16. (canceled) ~~The method of claim 14, wherein the portion of the hard mask which is left substantially intact comprises a silicon carbide SiC material.~~

17. (canceled) ~~A semiconductor device comprising an interconnect structure, the interconnect structure comprising:~~

~~an interlevel dielectric layer (ILD) layer having trenches filled with conductive material;~~

~~a hard mask overlying the interlevel dielectric layer (ILD); and~~

~~wherein at least a portion of the hard mask overlying the interlevel dielectric layer is substantially uniform in thickness and substantially planar irrespective of pattern density variations.~~

18. (canceled) ~~The semiconductor device of claim 17, wherein the conductive material is copper.~~

19. (canceled) ~~The semiconductor device of claim 17, wherein the portion of the hard mask comprises a silicon carbide (SiC) material.~~

20. (canceled) ~~The semiconductor device of claim 17, wherein:~~

~~the trenches are first overfilled with conductive material; and~~

~~processes used to remove excess conductive material substantially do not affect the portion of the hard mask overlying the interlevel dielectric layer.~~

Please insert the following:

21. (new) Method of forming an interconnect structure comprising the steps of:

depositing a dielectric layer comprising a material selected from the group consisting of low-k material and ultralow-k material;

forming a hard mask over the dielectric material, wherein the hard mask comprises:

a layer of silicon carbide (SiC) material overlying the dielecteric layer; and

a layer of oxide the silicon carbide material;

etching trenches in the dielectric material;

depositing a liner material over the hard mask and within the trenches; and

overfilling the trenches with a conductive material;

performing a first chemical mechanical polishing process to remove conductive material which is atop the liner, thereby exposing the liner;

removing that portion of the liner which is atop the hard mask using a process selected from the group consisting of reactive ion etch (RIE) and a Gas Cluster Ion Beam (GCIB), leaving conductive material protruding; and

removing the layer of oxide using a wet etch process, leaving the layer of silicon carbide, followed by performing a touch-up polishing process to remove conductive material protruding from the trenches.

22. (new) The method of claim 21, wherein:

the layer of silicon carbide material has a thickness in the range of 1000-5000A.

23. (new) The method of claim 21, wherein:

the layer of oxide has a thickness in the range of 1000-5000A.

24. (new) The method of claim 21, wherein the conductive material is copper.

25. (new) The method of claim 21, further comprising the step of:

ensuring that the layer of oxide is thick enough such that the topographical variations after

the first chemical mechanical polishing process and liner removal are entirely within the oxide portion of the hard mask.

26. (new) The method of claim 21, wherein the layer of oxide has a thickness in the range of 50 – 5000A.

27. (new) The method of claim 21, wherein the layer of silicon carbide material has a thickness in the range of 50 – 5000A.

28. (new) The method of claim 21, wherein the touch-up polishing process comprises using an abrasive-free or low-abrasive polish to obtain a very high selectivity between the conductive material and the second portion of the hard mask.